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(54) HIGH-LEVEL DATA LINK CONTROLLER(HDLC) RECEIVER STATE MACHINE

(57)Abstract:
PURPOSE: To obtain a receiver of a high level data link controller by perfoming flag and aboard detection, an intra-frame, external determination, zero elimination and several high level control functions with a signal logic device.
CONSTITUTION: A receiving FIFO buffer 49 contains a buffer of two word depth which connects a 8-bit shift register 46 to a data bus that includes a microprocessor interface. Each word, that is stored in the buffer 49 includes eight data bits and three state bits. That is, it includes FIFO location Fu 11 bits, CRC(cyclic redundancy check) bits and EOM(end-of-message) bits. Although each byte is loaded by the FIFO 49 when it is received by an HDLC receiver 40, it does not proceed until the next byte or an end flag is detected. A full bit and the EOM bit are set together when the end flag is detected, and when the CRC does not detects them, a CRC bit is invalidly set. When a state bit is set, a byte proceeds.